DATA REALIGNMENT TECHNIQUES FOR SERIAL-TO-PARALLEL CONVERSION

ABSTRACT OF THE DISCLOSURE

Techniques for adjusting the boundary between bytes of data in a serial-to-parallel converter are provided. Bits of serial data are shifted into a first register. Data bytes are then shifted out of the first register along parallel signal lines into a second register. The timing of the parallel load of data from the first register to the second register determines the parallel data byte boundary. The boundary between the parallel data bytes can be shifted using a load enable signal. The phase of the load enable signal can be changed to shift the boundary between data bytes by one or more bits. The parallel data can then be loaded from the second register into a third register. The data output signal of the third register is synchronized to a core clock signal to ensure enough set up and hold time for signals output by the third register.